

CPU:
AMD AM4
System Chipset:
Promontory A320 & B450
(Value DIY or System Builder)

CPU:

AMD AM4

System Chipset:

Promontory A320 & B450

(Value DIY or System Builder)

Main Memory:

DDR IV * 2 MAX:32 GB

VRM

UP9505 4+2

On Board Chipset:

LPC Super I/O --NCT5567

LAN RTL8111H

Azalia CODEC - Realtek ALC887

Expansion Slots:

From CPU

PCI Express X16 Slot * 1

PCI Express X1 Slot * 1

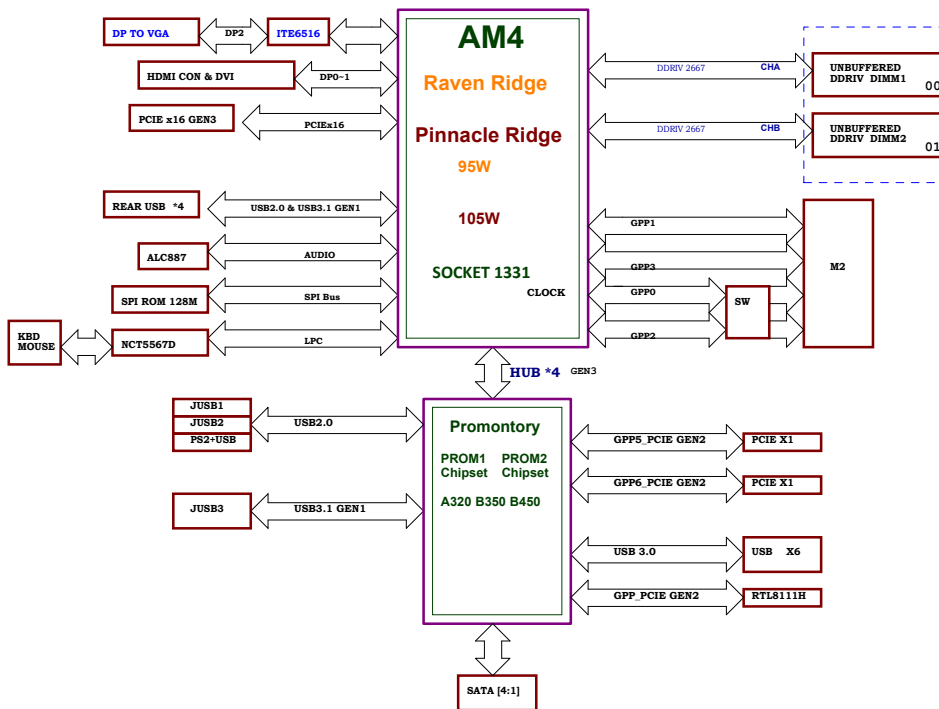
PCI Express X1 Slot * 1

M2 2 * 1


OCP IC:

RT9553B-Reserve

FUSION BLOCK DIAGRAM



01 Block Diagram	37 CPU Power VDDP-MP8712
02 Cover Sheet	38 CPU Power Connector/PWRGD
03 FM4 DDR4 I/F	39 CPU Power RT9505 4+2 Phase
04 AM4 PCIE/SATAE	40/41 CPU Power Phase 1-4
05 AM4 Display/Audio	42 CPU Power NB Phase 1-2
06 AM4 SVI/ACPI/GPIO	43 CPU Power NB Switch/NCT3933
07 AM4 LPC/SPI/USB/CLK/STRAP	44 RT9553B CURRENT SENSE
08 AM4 Power/RTC Power/ 09 AM4 GND	45 ATX/Front Panel
10,11 DDR4-DIMM CH-A/B	46 ALL LED Control
12,13 DDR4-POWER/GND	47 BOM Option
14 Promontory-PCIE/SATA/SATAE	48 RTC Circuit/Moat Cap
15 Promontory-USB/OC	49 M2_2
16 Promontory-CLK/ACPI/GPIO	50 History
17 Promontory-Power / 18 Promontory-GND	51 Power Sequence
19 PCIE X16(X1*2) SLOT	52 Power Delivery
20 SIO NCT5567D	53 GPIO MAP
21 DVI Connector	
22 CPU/SYS FAN Control TYPE K	
23 / 24 / 25 LAN-RTL8111H/Audio ALC887	
26 USB Rear PS2+USB2.0	
27 USB Rear LAN+USB3.1 GEN1	
28 USB Front Side	
29 SATA Connector	
30 HDMI Connector	
31 DP to VGA RTD2166	
32 ACPI uPI-5VDIMM&3VSB	
33 PM-SY8288RAC-1.05V/GS7133-2.5V	
34 DDR PWR VPP25/VT-TP-MP2147	
35 DDR Power-RT8231AGQW	
36 CPU Power 1P8V-MP2147	

**MSI**
Link to the Future

MICRO-START INTL CO.,LTD.

File

COVER SHEET

Size

Document Number

Rev

Custom

MS-7B84

22

Date

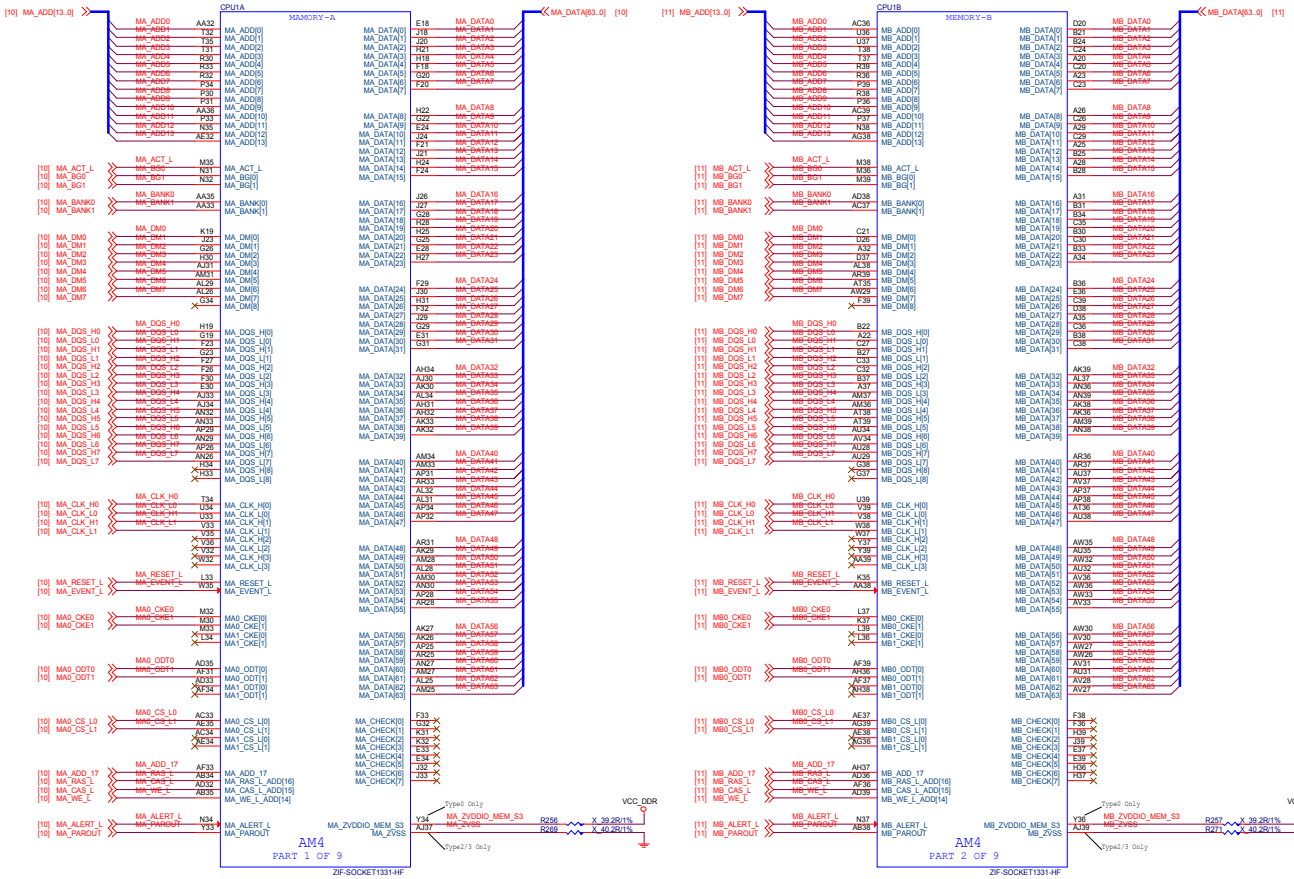
Friday, July 15, 2016

Sheet

2

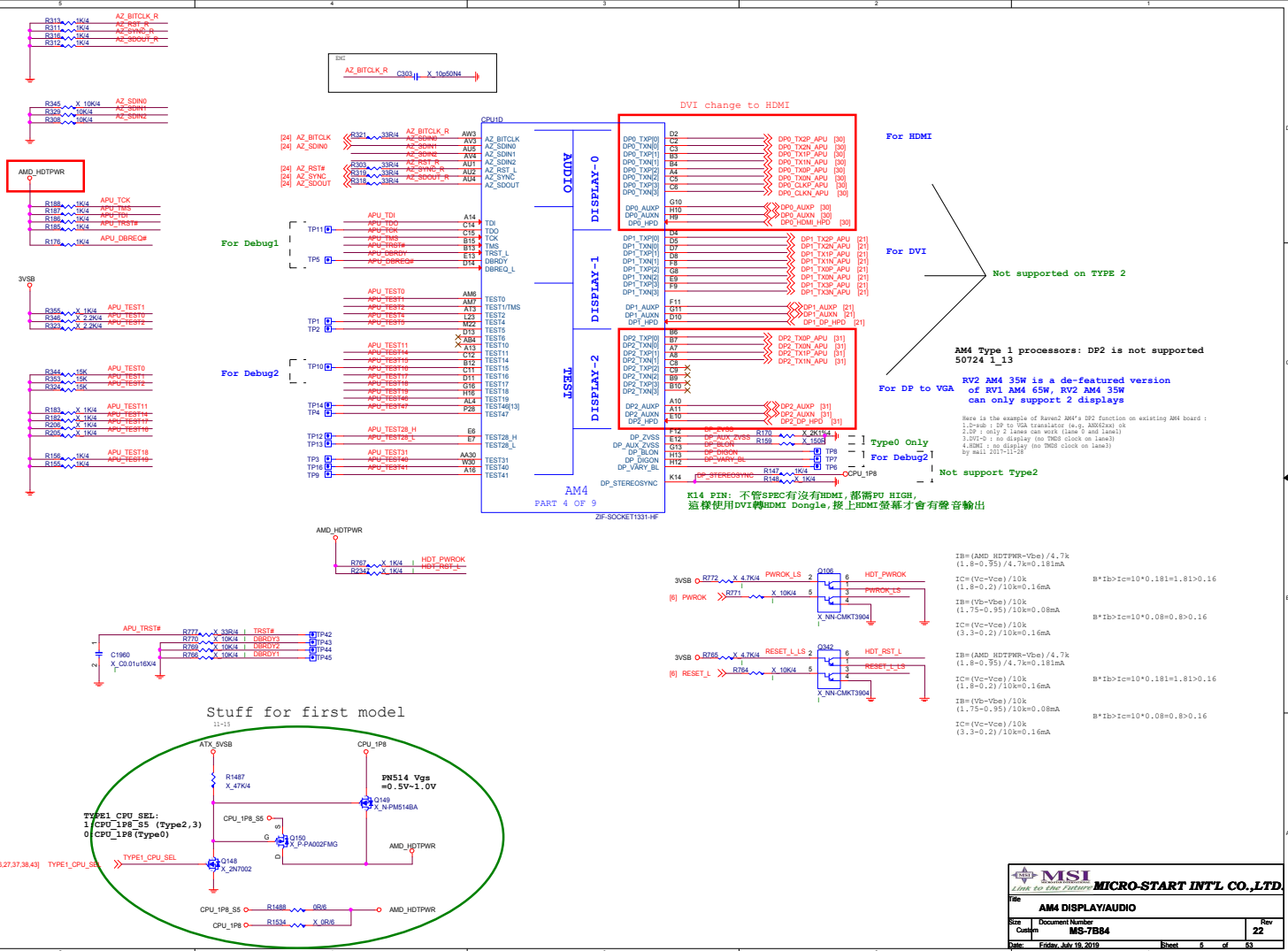
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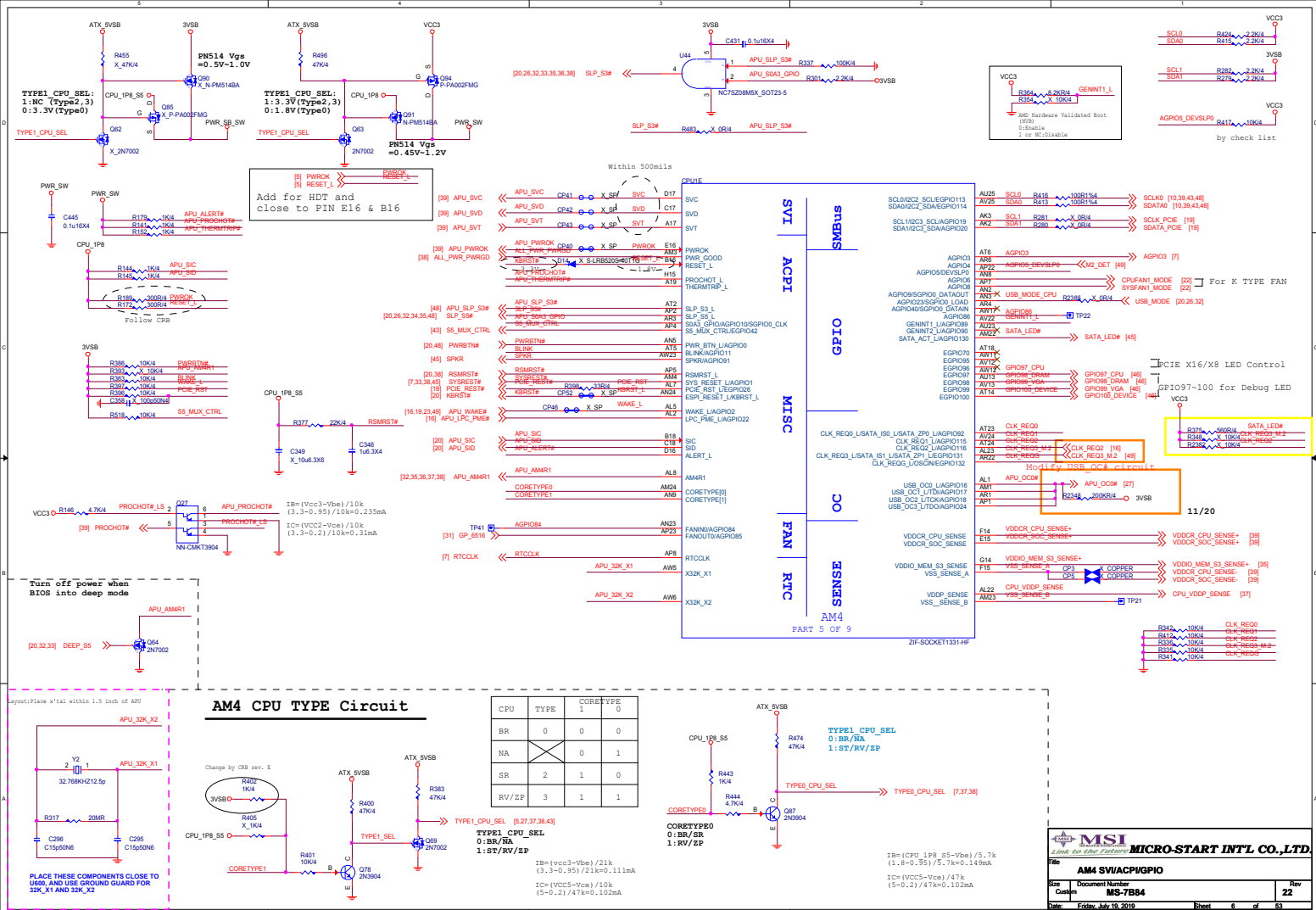
53



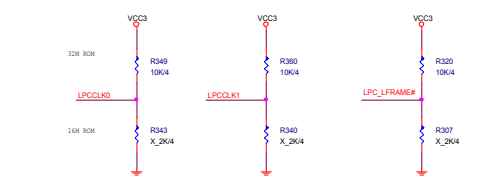
Schematic Cfg	Project
	V A

MSI MICRO-START INTL CO., LTD.		
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File	AM4 DDR4 IF	
Size	Document Number	New
Custom	MS-7B84	22
Date	Friday, July 16, 2010	Sheet 3 of 53

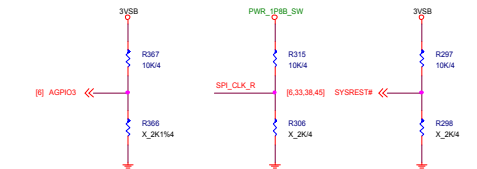




Strapping Options



	LPCCLK0	LPCCLK1	SIO_LFRAME
PULL HIGH	LPC device Boot Fail Timer Enabled	Configured for Internal clock generator	SPI ROM
		(Default)	(Default)
PULL LOW	LPC device Boot Fail Timer Disabled	Configured for External clock generator	LPC ROM
	(Default)	????	



	AGPIO3	SPI_CLK	SYSREST#
PULL HIGH	Enhanced Reset logic	Use 48Mhz crystal clock and generate both internal and external clocks	Normal reset mode
	(Default)	(Default)	(Default)
PULL LOW	Traditional Reset logic	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode

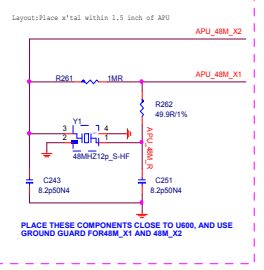
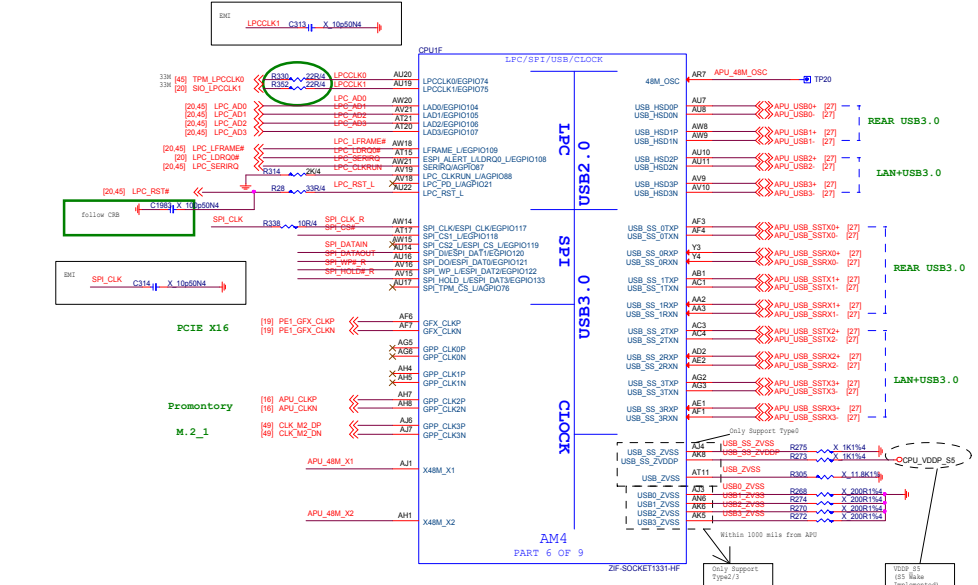
	RTCCLK
PULL HIGH	RTC Coin Battery is on board
	(Default)
PULL LOW	RTC Coin Battery is not on board

MSI MICRO-START INTL CO., LTD.

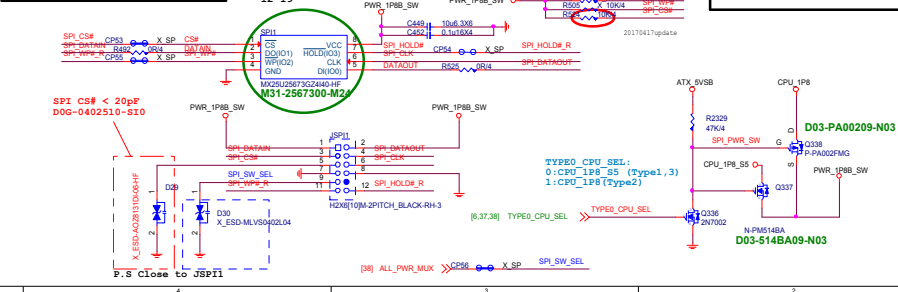
File: AM4 LPC/SPU/USB/CLK/STRAP

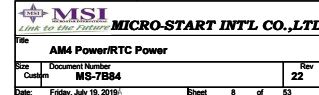
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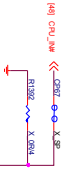
Date: Friday, July 15, 2016 Sheet: 7 of 53



SPI ROM (1.8V)

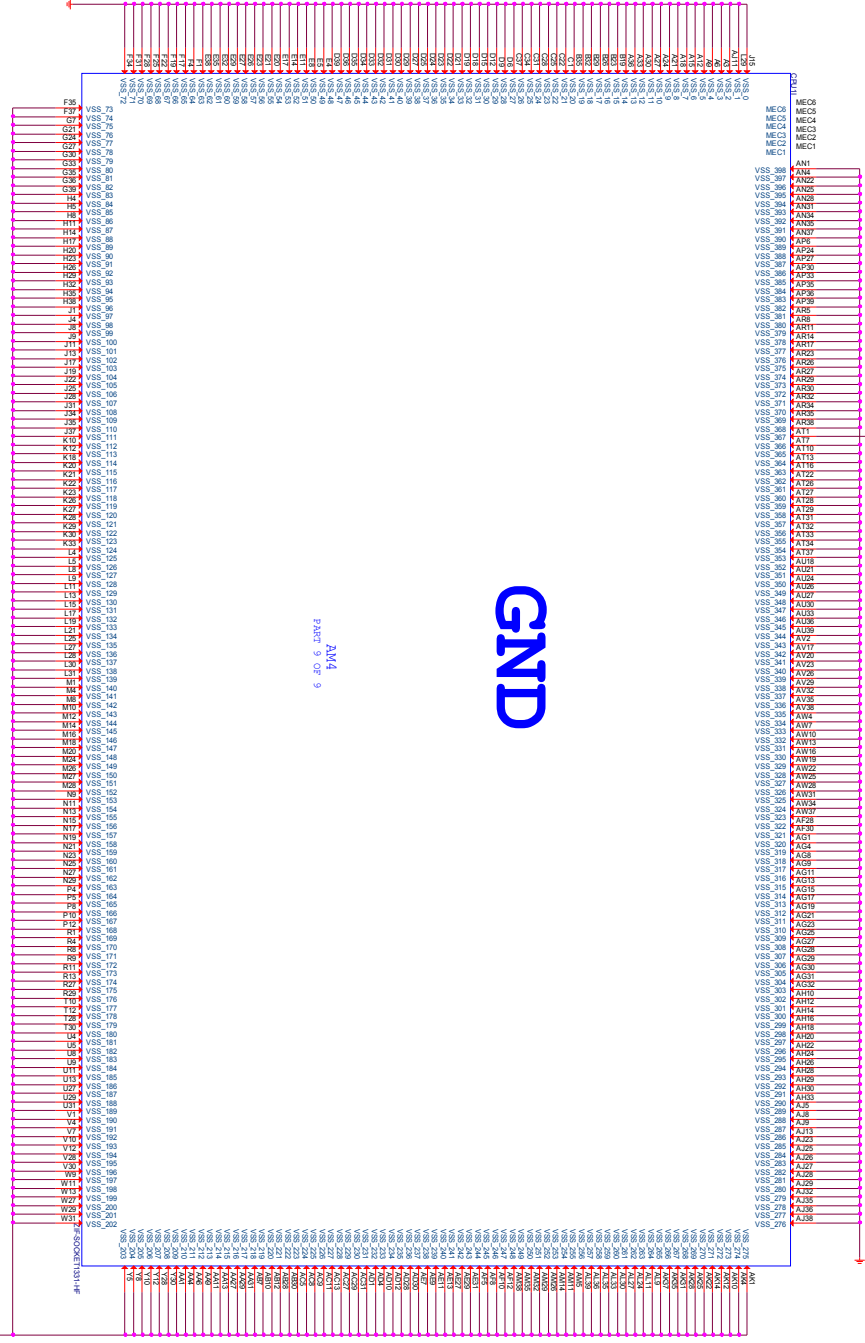







GND

AM4
PART 9 OF 9



**MSI**
MIcro-STARt INTEL CO., LTD.

TO

AM4 GND

FROM

MS-7B34

Rev

22

Form

AM4-2013

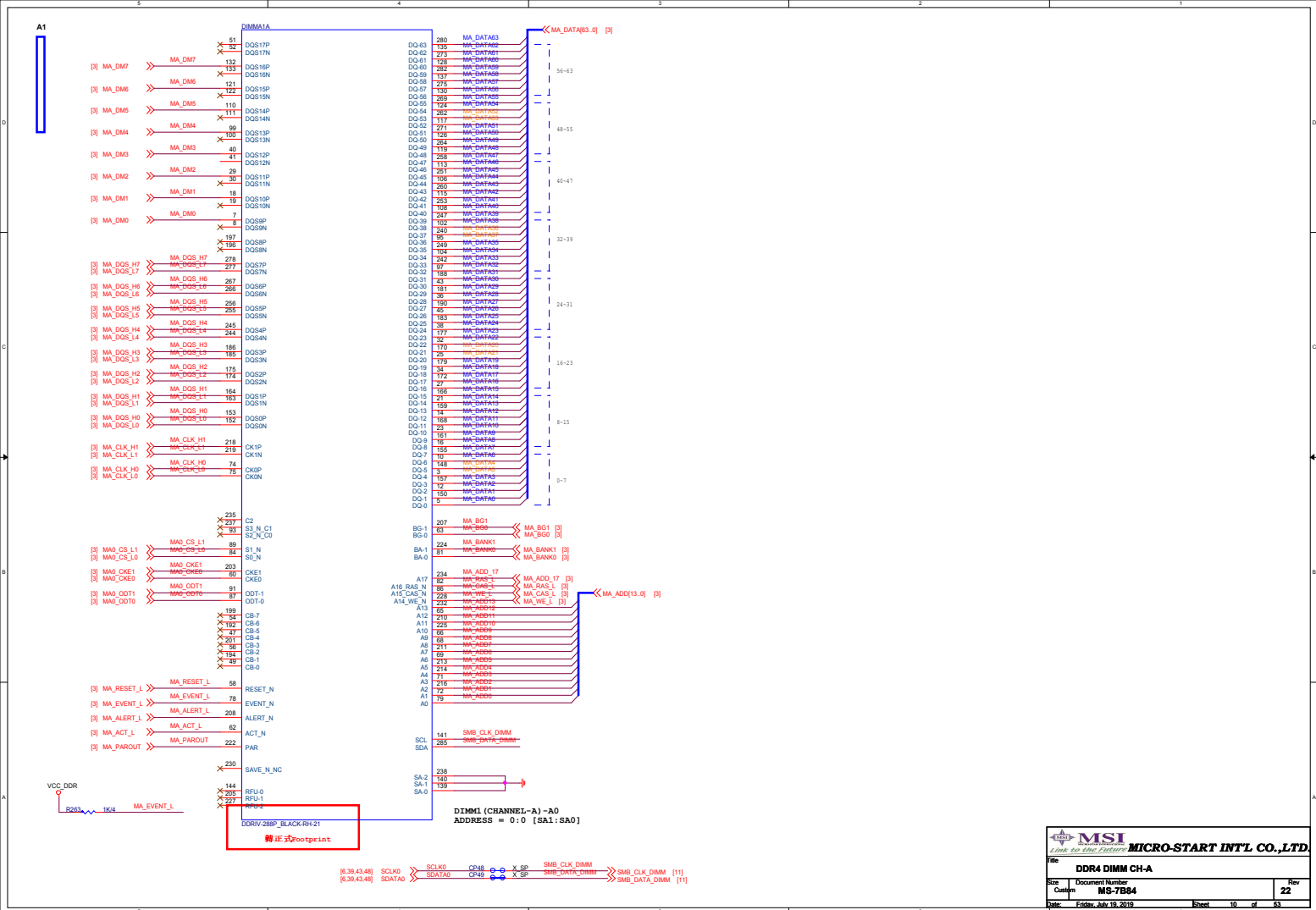
Board

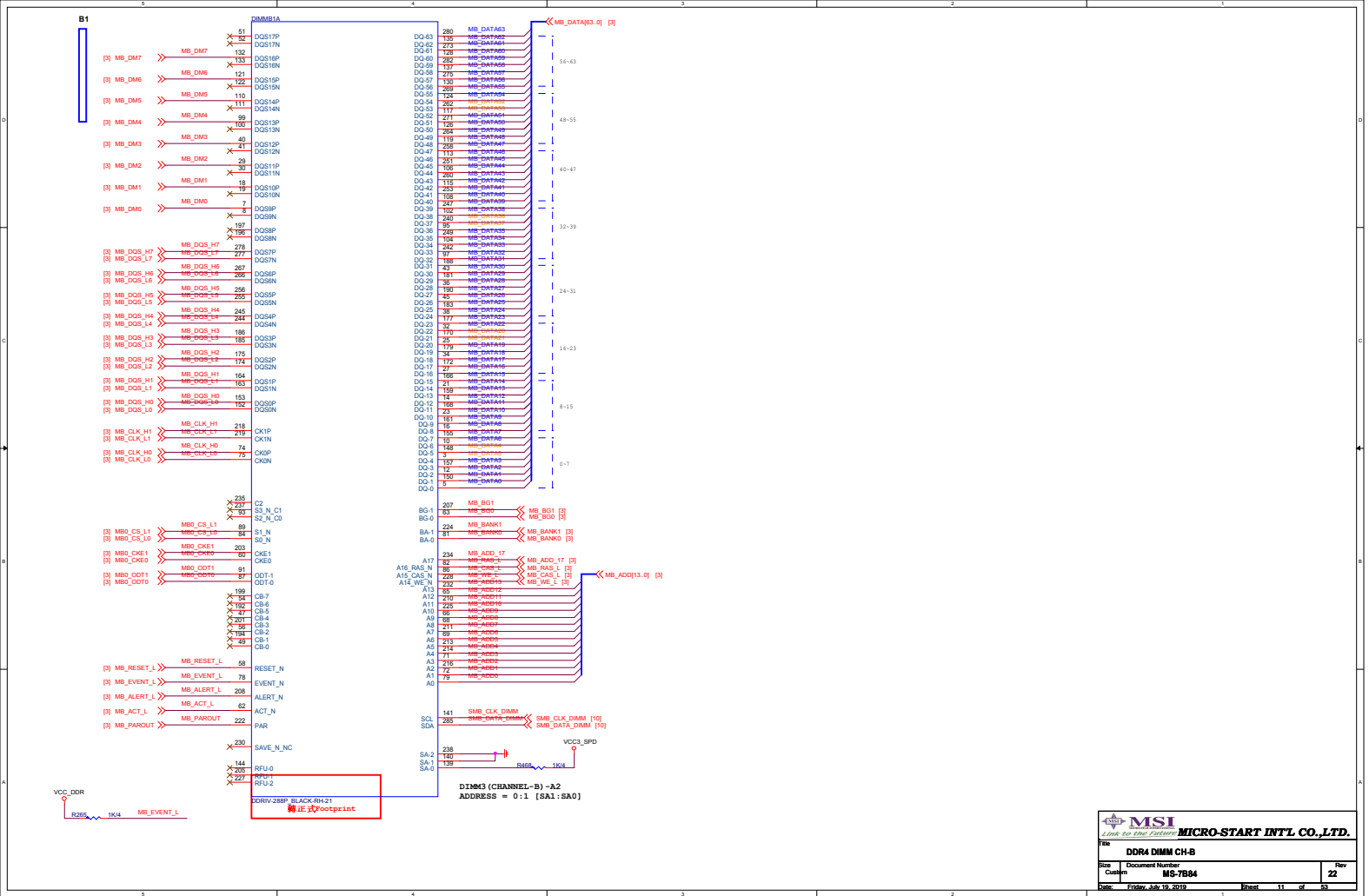
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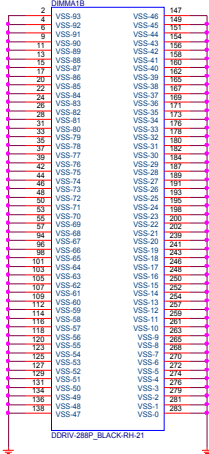
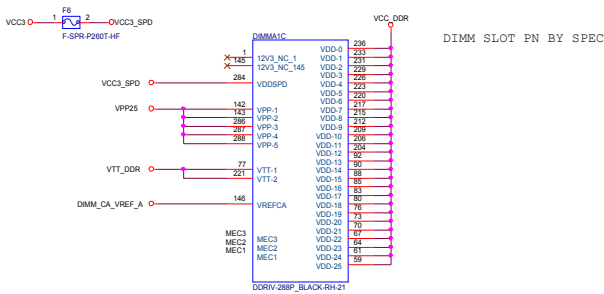
Doc

53

5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103 104 105 106 107 108 109 110 111 112 113 114 115 116 117 118 119 120 121 122 123 124 125 126 127 128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 148 149 150 151 152 153 154 155 156 157 158 159 160 161 162 163 164 165 166 167 168 169 170 171 172 173 174 175 176 177 178 179 180 181 182 183 184 185 186 187 188 189 190 191 192 193 194 195 196 197 198 199 200 201 202 203 204 205 206 207 208 209 210 211 212 213 214 215 216 217 218 219 220 221 222 223 224 225 226 227 228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250 251 252 253 254 255 256 257 258 259 260 261 262 263 264 265 266 267 268 269 270 271 272 273 274 275 276 277 278 279 280 281 282 283 284 285 286 287 288 289 290 291 292 293 294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316 317 318 319 320 321 322 323 324 325 326 327 328 329 330 331 332 333 334 335 336 337 338 339 340 341 342 343 344 345 346 347 348 349 350 351 352 353 354 355 356 357 358 359 360 361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384 385 386 387 388 389 390 391 392 393 394 395 396 397 398 399 400 401 402 403 404 405 406 407 408 409 410 411 412 413 414 415 416 417 418 419 420 421 422 423 424 425 426 427 428 429 430 431 432 433 434 435 436 437 438 439 440 441 442 443 444 445 446 447 448 449 450 451 452 453 454 455 456 457 458 459 460 461 462 463 464 465 466 467 468 469 470 471 472 473 474 475 476 477 478 479 480 481 482 483 484 485 486 487 488 489 490 491 492 493 494 495 496 497 498 499 500 501 502 503 504 505 506 507 508 509 510 511 512 513 514 515 516 517 518 519 520 521 522 523 524 525 526 527 528 529 530 531 532 533 534 535 536 537 538 539 540 541 542 543 544 545 546 547 548 549 550 551 552 553 554 555 556 557 558 559 560 561 562 563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582 583 584 585 586 587 588 589 590 591 592 593 594 595 596 597 598 599 600 601 602 603 604 605 606 607 608 609 610 611 612 613 614 615 616 617 618 619 620 621 622 623 624 625 626 627 628 629 630 631 632 633 634 635 636 637 638 639 640 641 642 643 644 645 646 647 648 649 650 651 652 653 654 655 656 657 658 659 660 661 662 663 664 665 666 667 668 669 670 671 672 673 674 675 676 677 678 679 680 681 682 683 684 685 686 687 688 689 690 691 692 693 694 695 696 697 698 699 700 701 702 703 704 705 706 707 708 709 710 711 712 713 714 715 716 717 718 719 720 721 722 723 724 725 726 727 728 729 730 731 732 733 734 735 736 737 738 739 740 741 742 743 744 745 746 747 748 749 750 751 752 753 754 755 756 757 758 759 760 761 762 763 764 765 766 767 768 769 770 771 772 773 774 775 776 777 778 779 780 781 782 783 784 785 786 787 788 789 790 791 792 793 794 795 796 797 798 799 800 801 802 803 804 805 806 807 808 809 810 811 812 813 814 815 816 817 818 819 820 821 822 823 824 825 826 827 828 829 830 831 832 833 834 835 836 837 838 839 840 841 842 843 844 845 846 847 848 849 850 851 852 853 854 855 856 857 858 859 860 861 862 863 864 865 866 867 868 869 870 871 872 873 874 875 876 877 878 879 880 881 882 883 884 885 886 887 888 889 890 891 892 893 894 895 896 897 898 899 900 901 902 903 904 905 906 907 908 909 910 911 912 913 914 915 916 917 918 919 920 921 922 923 924 925 926 927 928 929 930 931 932 933 934 935 936 937 938 939 940 941 942 943 944 945 946 947 948 949 950 951 952 953 954 955 956 957 958 959 960 961 962 963 964 965 966 967 968 969 970 971 972 973 974 975 976 977 978 979 980 981 982 983 984 985 986 987 988 989 990 991 992 993 994 995 996 997 998 999 1000

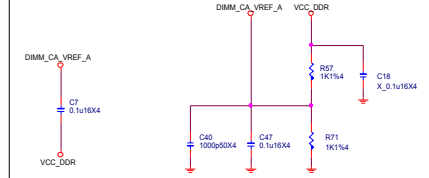


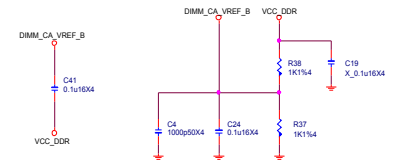
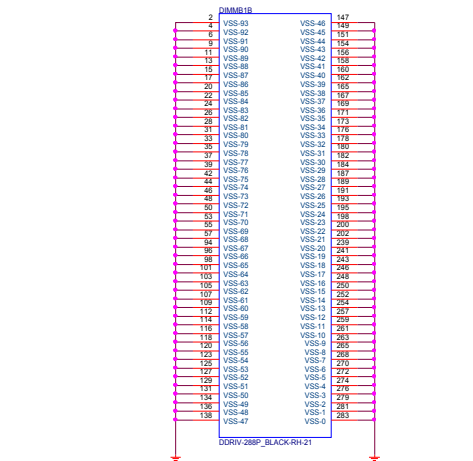





DDR VREF

(place resistors close to DIMMs)



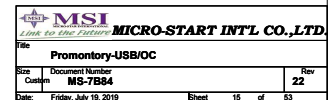


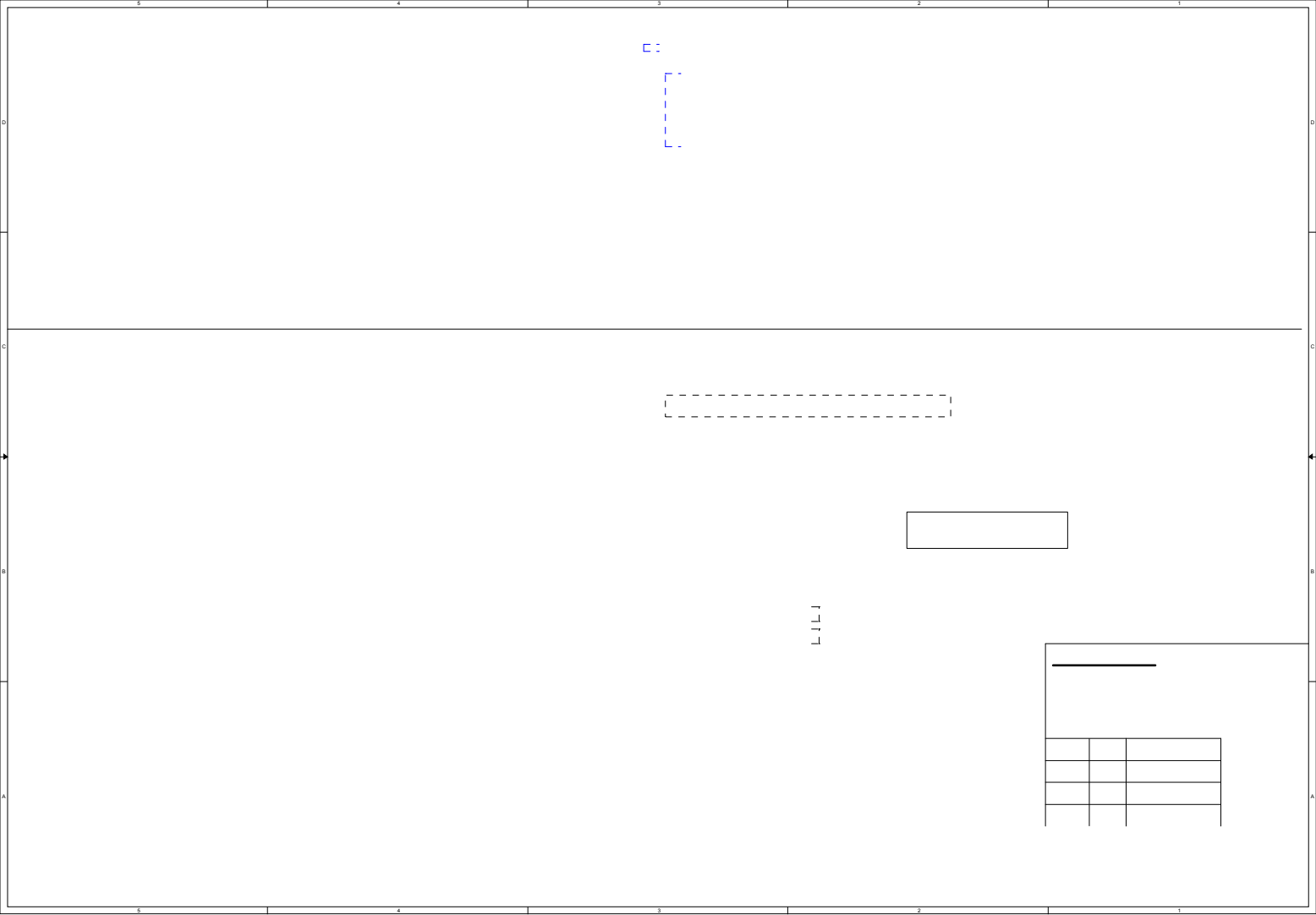
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Title DDR4-POWER/GND-2							
Size Custom		Document Number MS-7B84				Rev 22	
Date: Friday, July 19, 2019		Sheet 13		of 53			

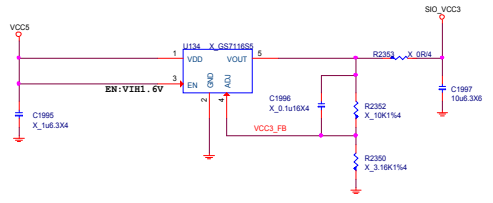
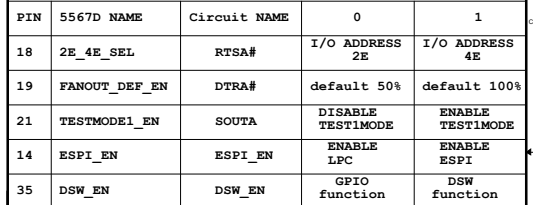
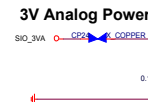
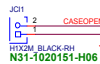
USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	USB2.0	USB_OC
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_HSDP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0-1	USB_SS Port 0-5	USB_HSD Port0-13	USB_SSP Port0
PROM2	USB_SSP Port0-1	USB_SS Port 0-1	USB_HSD Port0-5 USB_HSD Port10-13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0-5 USB_HSD Port10, 12-13	USB_SSP Port0

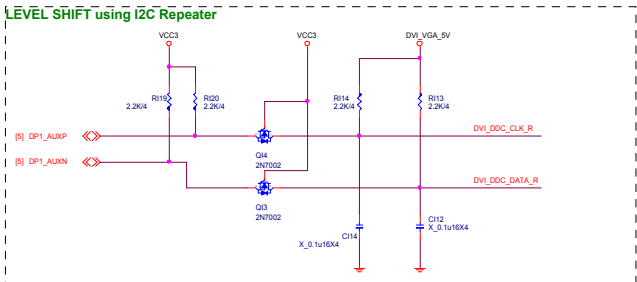
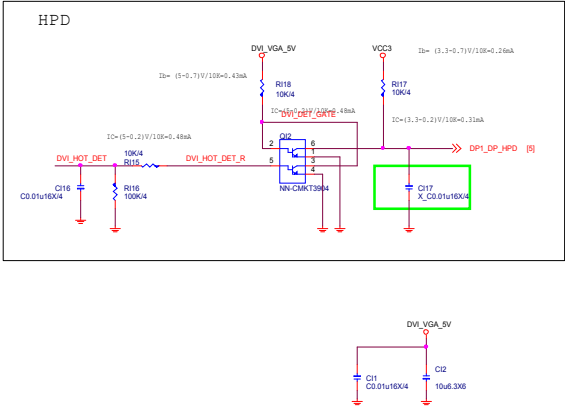
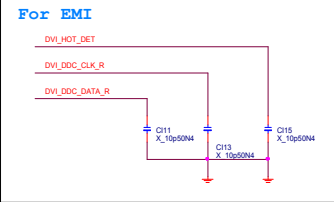
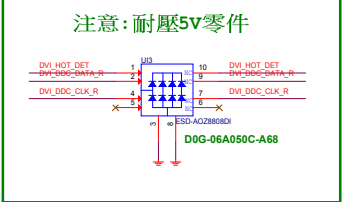
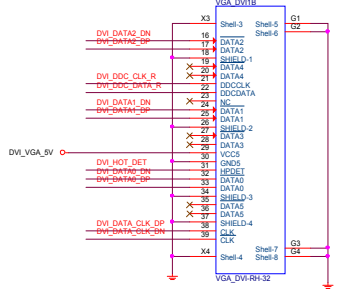
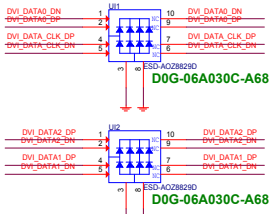
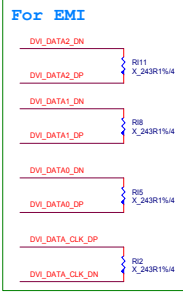
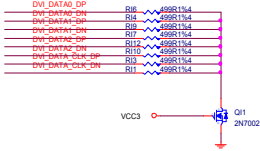
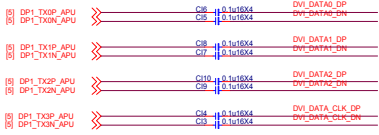
CLK2.3不能用
CLK1-3不能用






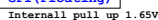
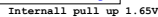
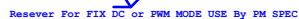


DVI CONNECTOR



 MSI <small>Micro-Star International, Inc.</small> <i>Link to the Future</i>		MICRO-START INT'L CO., LTD	
Title DVI			
Size	Document Number		Rev
Custom	MS-7B84		22
Date:	Friday, July 19, 2019	Sheet	21 of 53


2. GPIO可以由BIOS切換 PWM/DC MODE



[illegible]

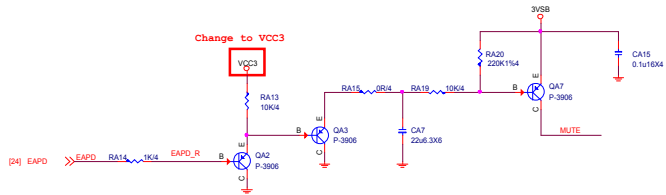
	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

 MSI <small>Micro-Star International Co., Ltd.</small> <i>Link to the Future</i>				MICRO-START INT'L CO.,LTD.			
Title LAN-RTL8111H							
Size Custom		Document Number MS-7B84				Rev 22	
Date: Friday, July 19, 2019		Sheet 23		of 53			

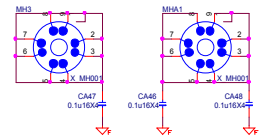
Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)

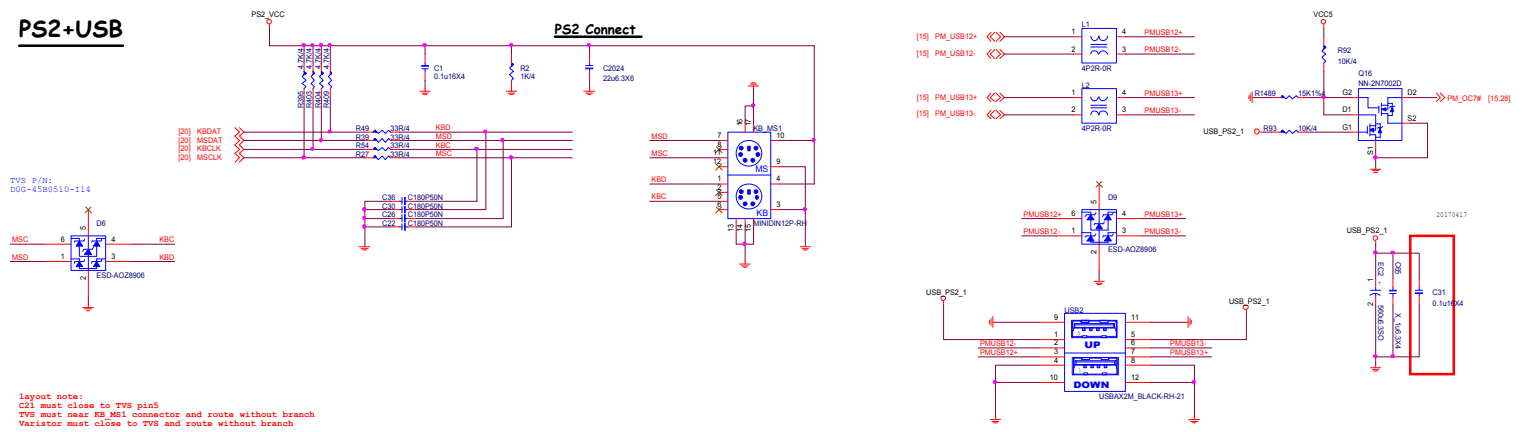


Digital

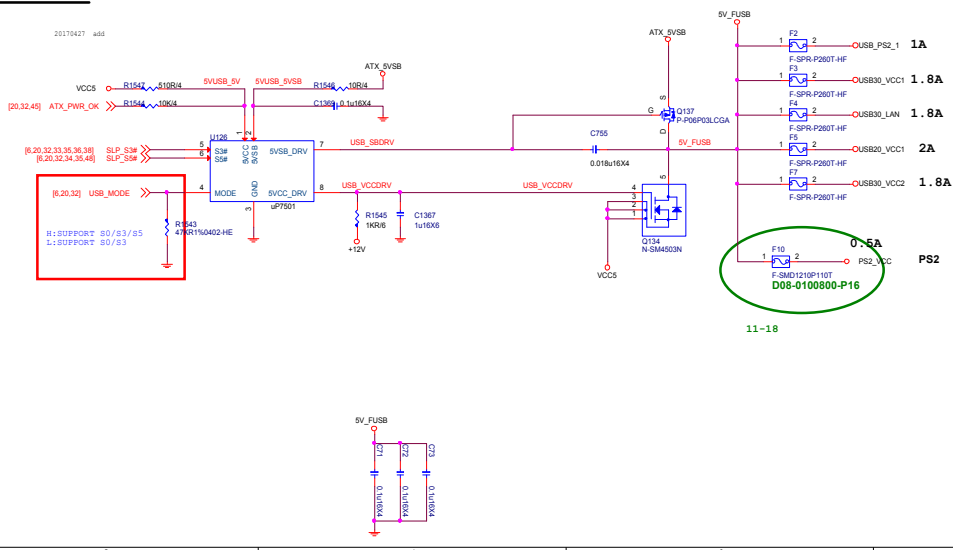
Analog




PS2+USB

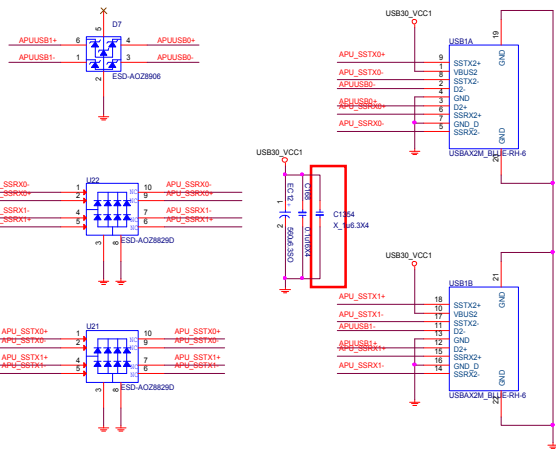
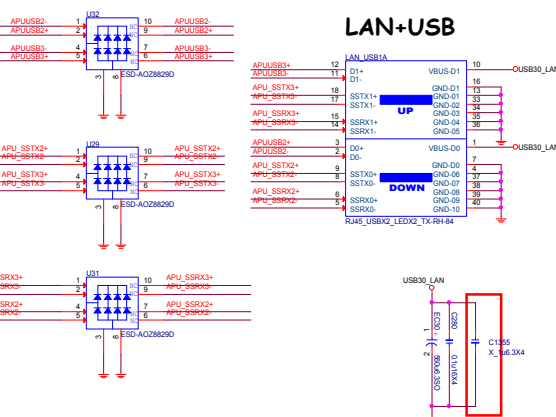


USB Power



 MSI <i>Link to the Future</i>				MICRO-START INT'L CO.,LTD.			
Title USB Rear PS2+USB2.0							
Size Custom		Document Number MS-7B84				Rev 22	
Date: Friday, July 19, 2019				Sheet 26 of 53			

[7] $\text{APU_USB_SSTX}0+ \xrightarrow{\text{C181}} 0.226/3X4 \text{ APU_SSTX}0+$
 [7] $\text{APU_USB_SSTX}0- \xrightarrow{\text{C181}} 0.226/3X4 \text{ APU_SSTX}0-$
 [7] $\text{APU_USB_SSRX}0+ \xrightarrow{\text{C184}} 0.33/6/3X4 \text{ APU_SSRX}0+$
 [7] $\text{APU_USB_SSRX}0- \xrightarrow{\text{C184}} 0.33/6/3X4 \text{ APU_SSRX}0-$
 [7] $\text{APU_USB}0+ \xrightarrow{\text{APU_USB}0+} \text{APR}0 \text{ OR} \text{ APU_USB}0+ \text{ APU_USB}0+$
 [7] $\text{APU_USB}0- \xrightarrow{\text{APU_USB}0-} \text{APR}0 \text{ OR} \text{ APU_USB}0- \text{ APU_USB}0-$
 [7] $\text{APU_USB}1+ \xrightarrow{\text{APU_USB}1+} \text{APR}1 \text{ OR} \text{ APU_USB}1+ \text{ APU_USB}1+$
 [7] $\text{APU_USB}1- \xrightarrow{\text{APU_USB}1-} \text{APR}1 \text{ OR} \text{ APU_USB}1- \text{ APU_USB}1-$
 [7] $\text{APU_USB_SSTX}1+ \xrightarrow{\text{C185}} 0.226/3X4 \text{ APU_SSTX}1+$
 [7] $\text{APU_USB_SSTX}1- \xrightarrow{\text{C187}} 0.226/3X4 \text{ APU_SSTX}1-$
 [7] $\text{APU_USB_SSRX}1+ \xrightarrow{\text{C188}} 0.33/6/3X4 \text{ APU_SSRX}1+$
 [7] $\text{APU_USB_SSRX}1- \xrightarrow{\text{C189}} 0.33/6/3X4 \text{ APU_SSRX}1-$

[illegible]

Modify USB_OC# circuit

USB_XORO

3V5B

R483
200K/R4

U25

5.6,37,38,43 TYPE1_CPU_SEL

APU_OC0# [R]

SN74VLC1G85DCKR_SC70-5 RH

VCC5

R1483
15K/R4

R394
10K/R4

Q32
SN-2N7002SD

USB30_VCC1

R177
10K/R4

REC02+USB (USB3.0)

USB30_VCC1

VCC5

R394
10K/R4

R1483
15K/R4

Q75
SN-2N7002SD

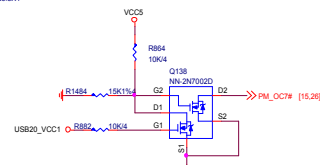
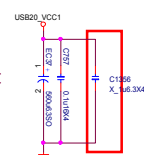
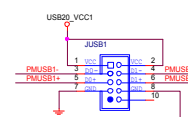
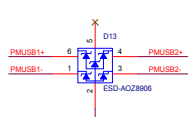
USB30_LAN

R376
10K/R4

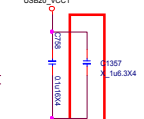
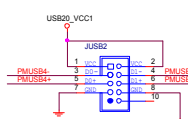
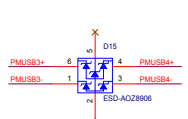
LAN+USB (USB3.0)

	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

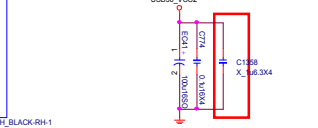
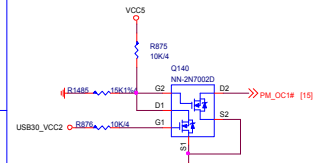
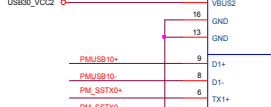
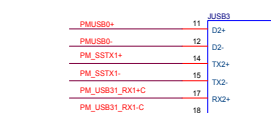
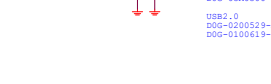
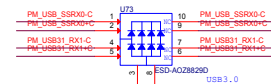
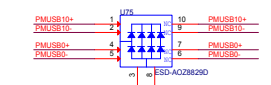
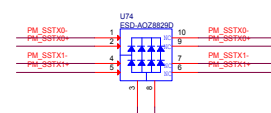
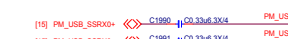
5V@1A



5V@1A



[15] PM_USB_SSTX0+ <<> C760 0.22uF 3X4 PM_SSTX0+
[15] PM_USB_SSTX0- <<> C759 0.22uF 3X4 PM_SSTX0-



```

290
USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL

USB2.0
D0G-0200529-A68 Main
D0G-0100610-I05 AVL

```

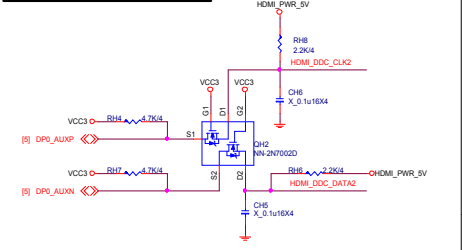
SATA Connector



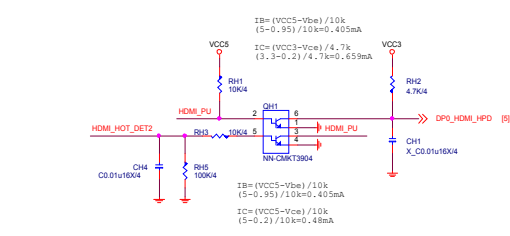
HDMI CONNECTOR

For HDMI 1.4

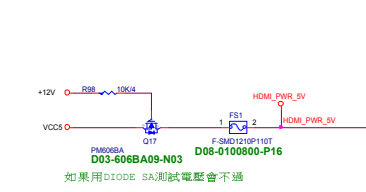
AUX Level Shifter



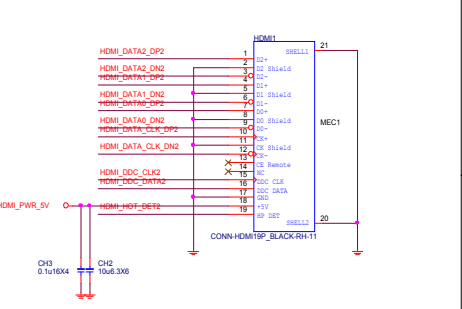
HPD Circuit



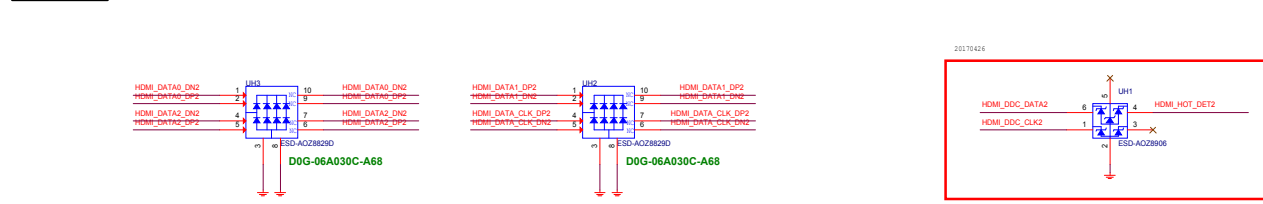
Connector Power



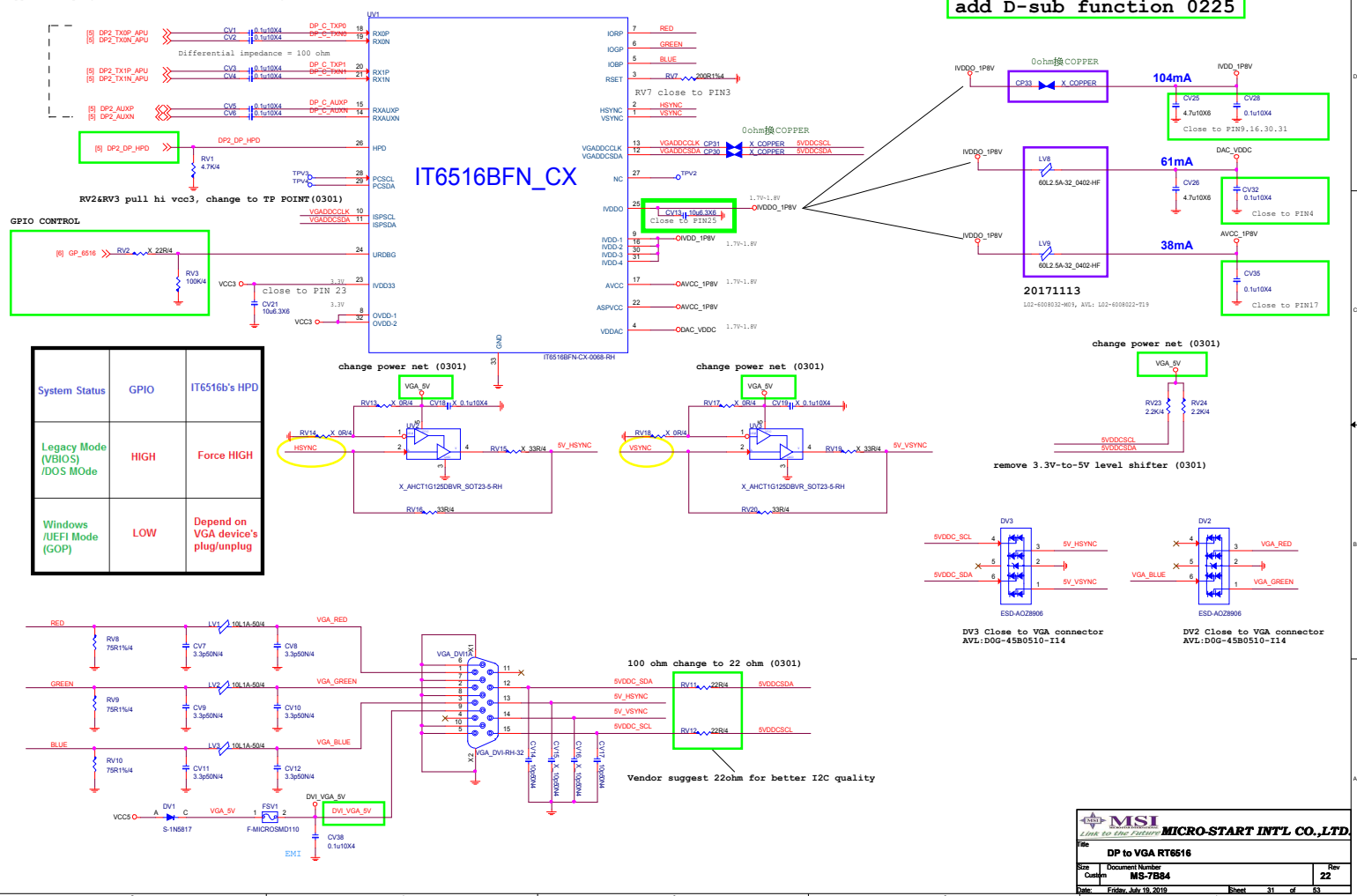
Connector



For EMI



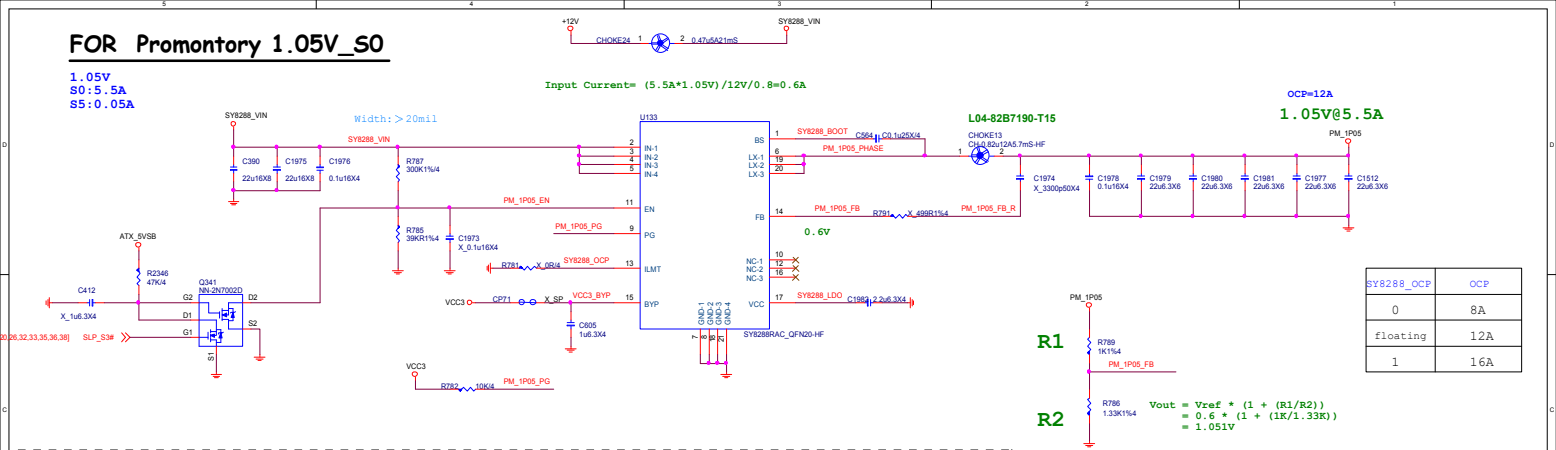
Note:
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



[illegible][illegible]

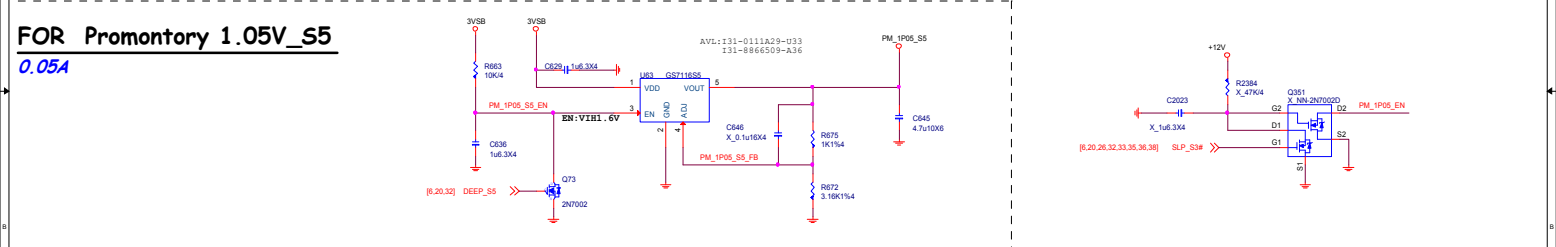
FOR Promontory 1.05V_S0

1.05V
S0:5.5A
S5:0.05A



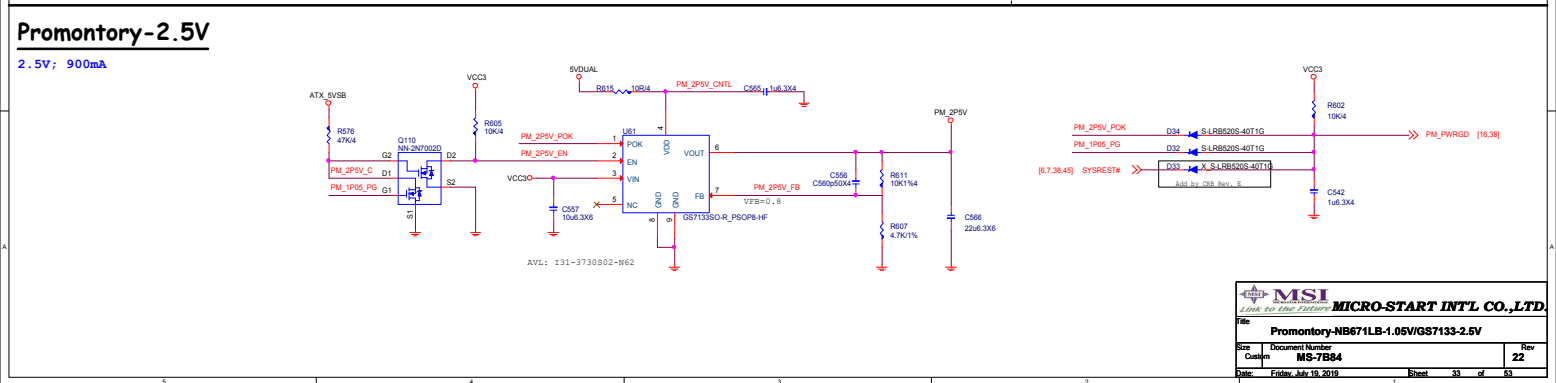
FOR Promontory 1.05V_S5

0.05A

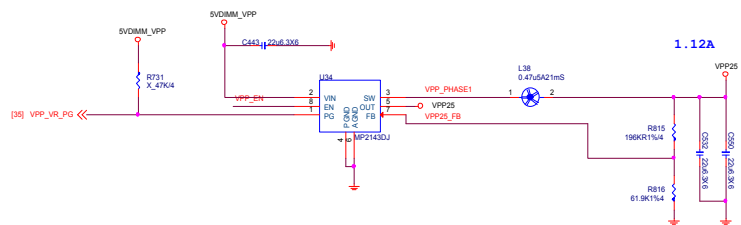
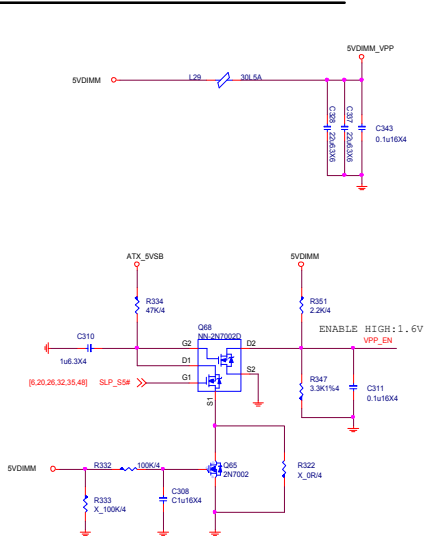


Promontory-2.5V

2.5V; 900mA

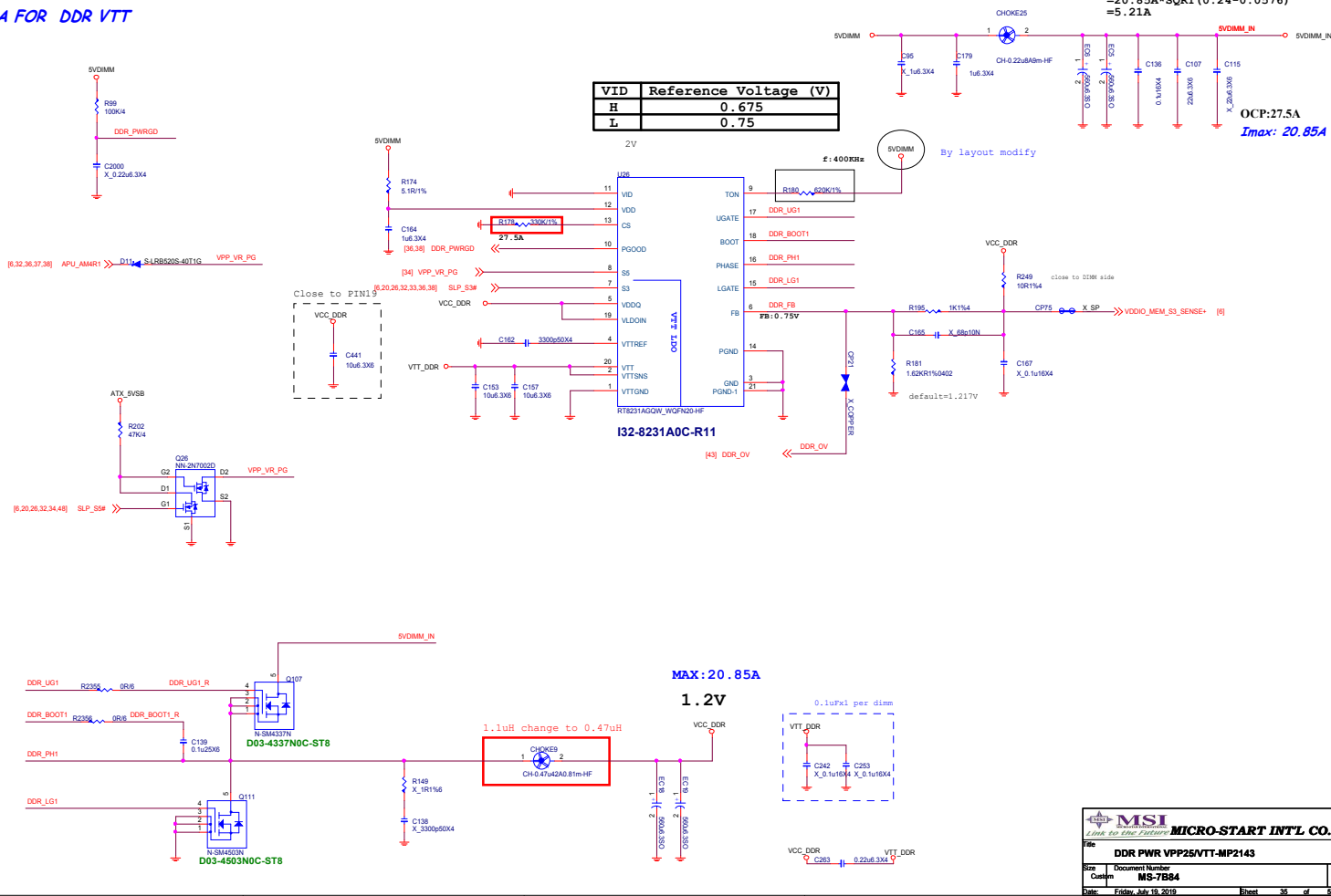


2DIMM :1.12A FOR DDR VPP2.5V



15.5A FOR CPU
4.75A FOR 2DIMM
0.6A FOR DDR VTT

```
Irms = Iout * SQRT{D/N- (D)^2}
VCCDDR:
D=Vout/Vin=1.2/5=0.24
N=Phase number=1
=20.85A*SQRT(0.24-0.0576)
=5.21A
```



FOR CPU 1.8V S5

0.5A

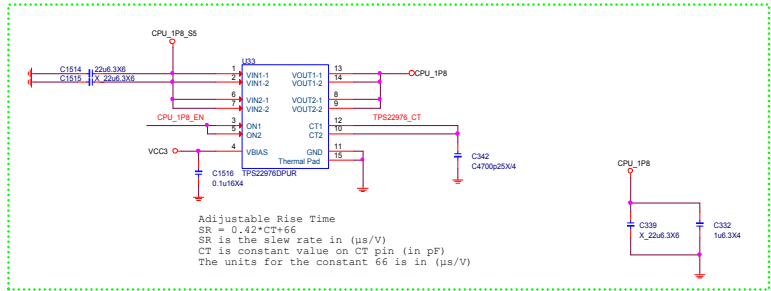
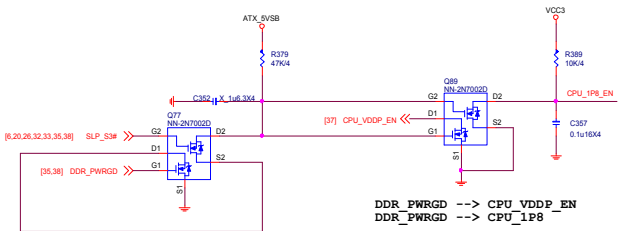
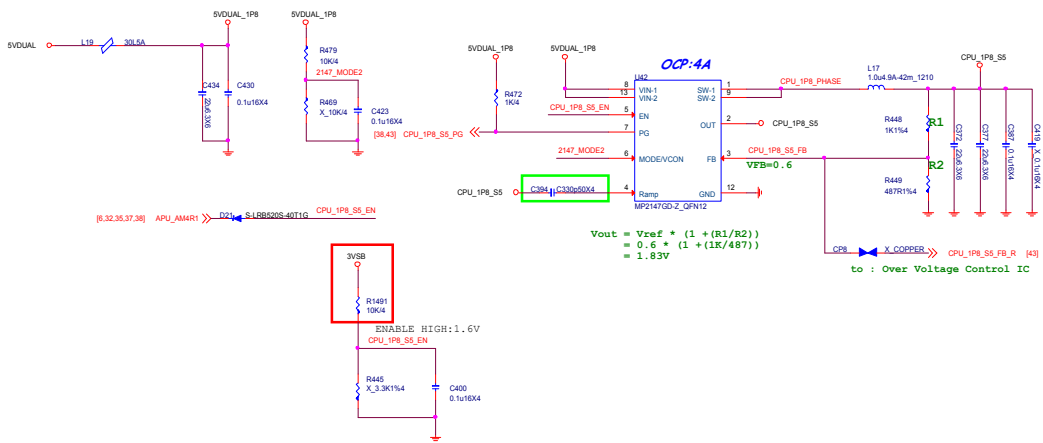
FOR VCCP_SOC_S5

0.9A

FOR CPU 1.8V S0

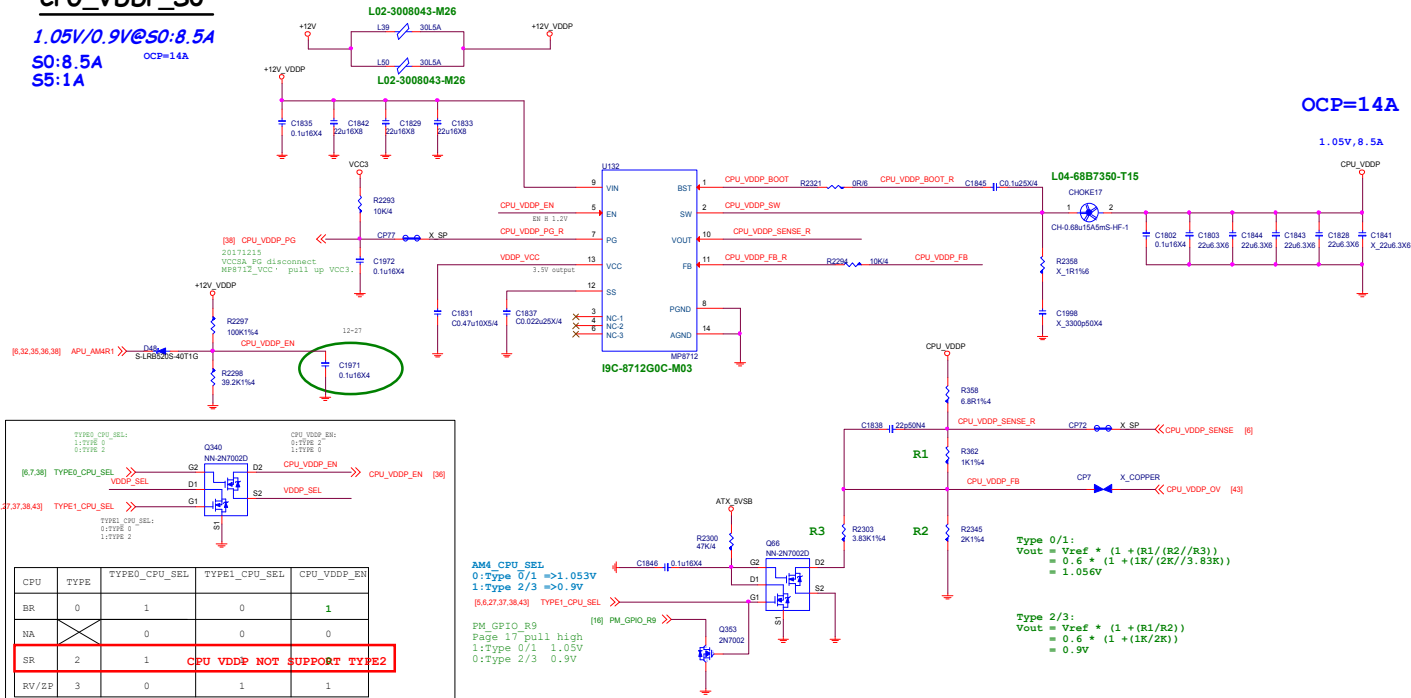
2.0A

$0.5A + 2.0A + 0.9A = 3.4A$



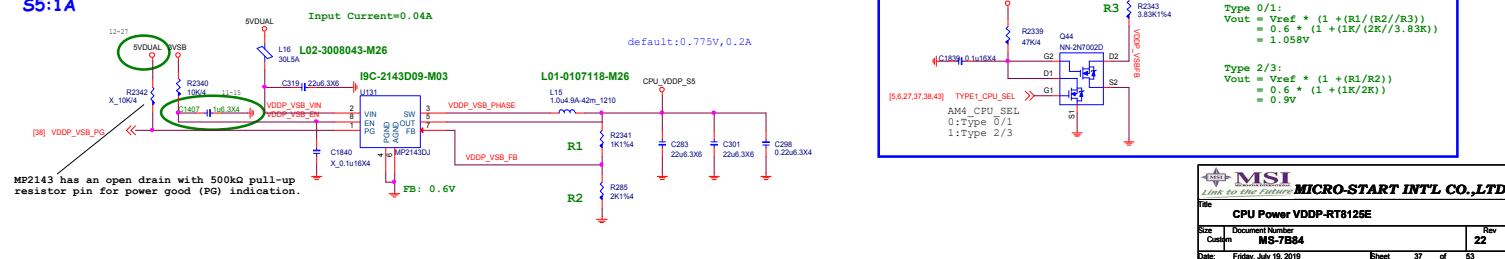
1.05V/0.9V@S0:8.5A
S0:8.5A OCP=14A
S5:1A

OCP=14A

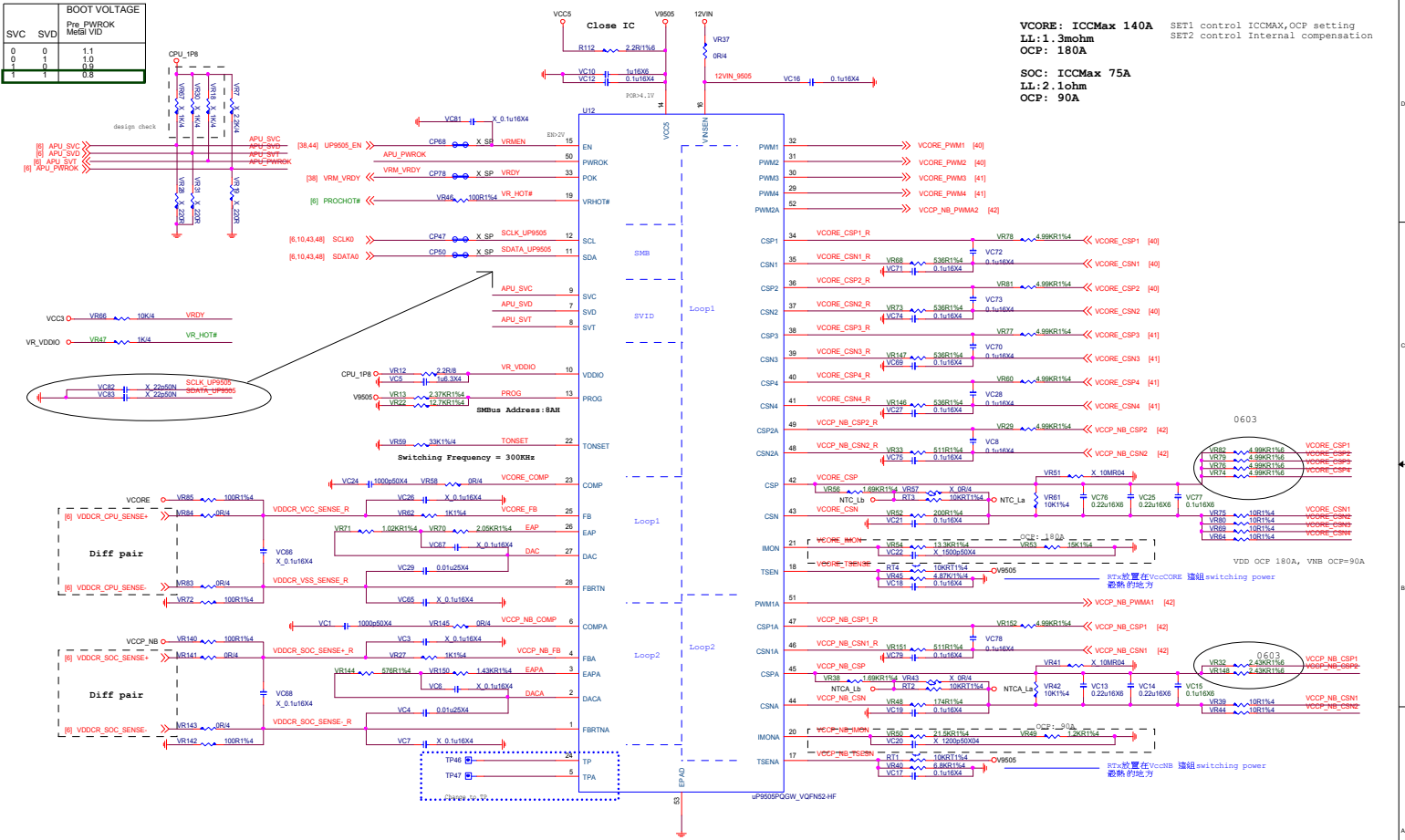


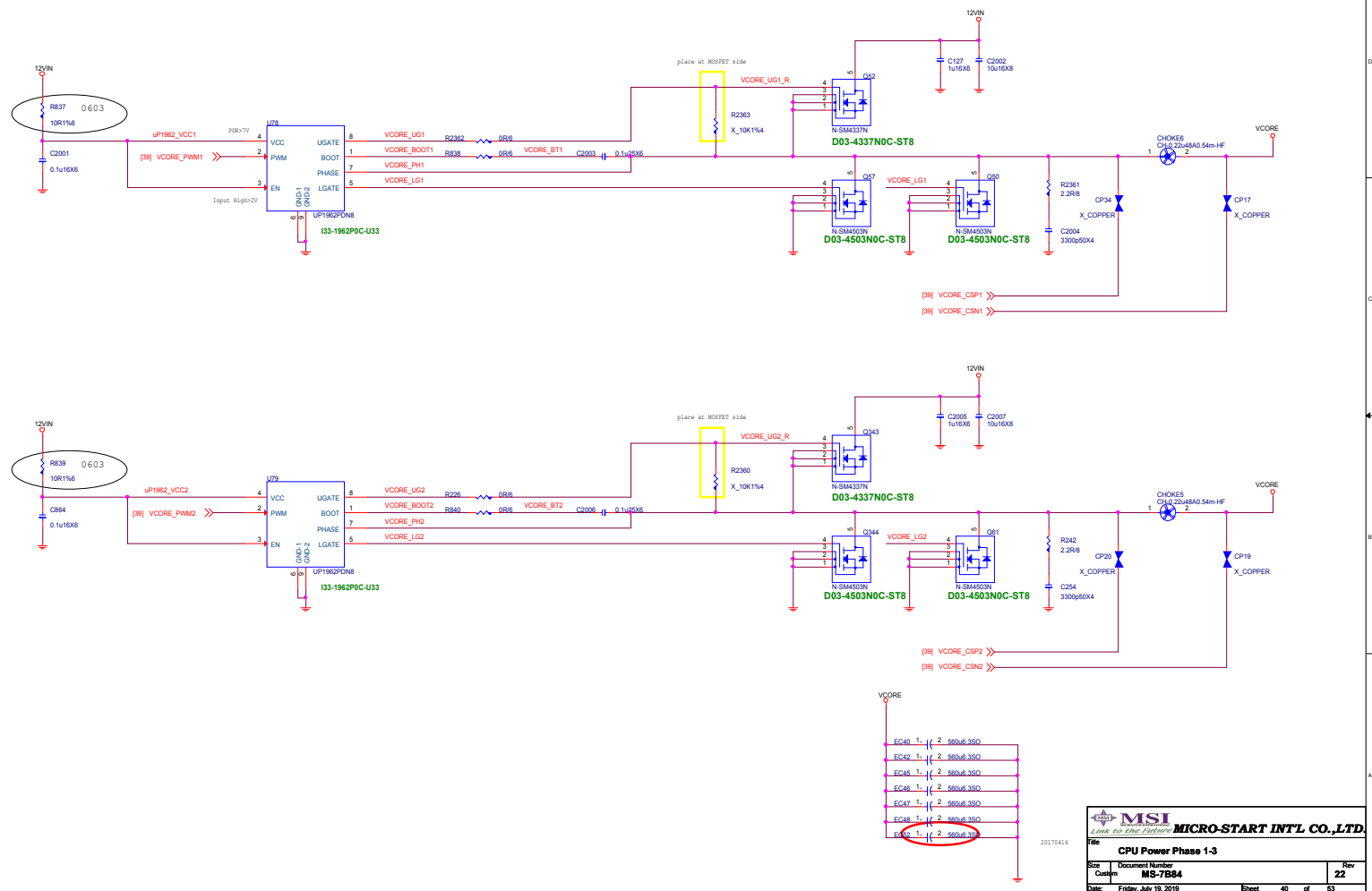
1.05V/0.9V
S5:1A

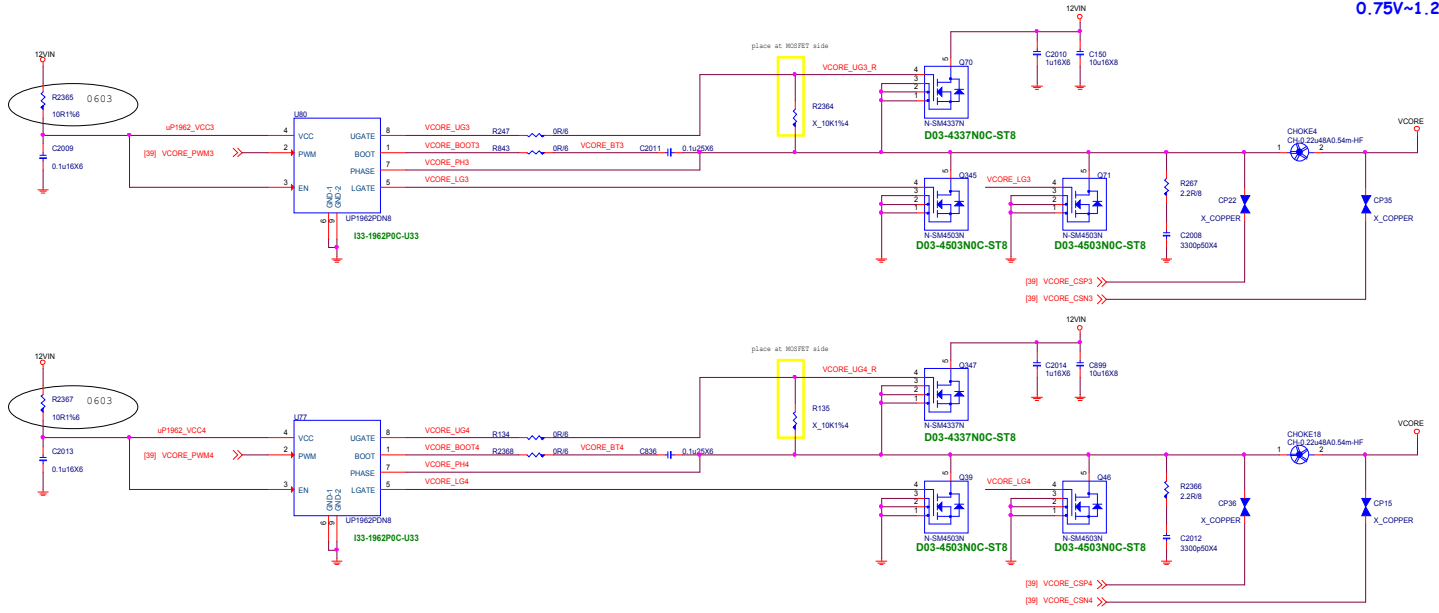
default:0.775V,0.2A



BOOT VOLTAGE		Pre_PWROK
SVC	SVD	Metal VID
0	0	1.1
0	1	1.0
0	0	0.9
1	1	0.8





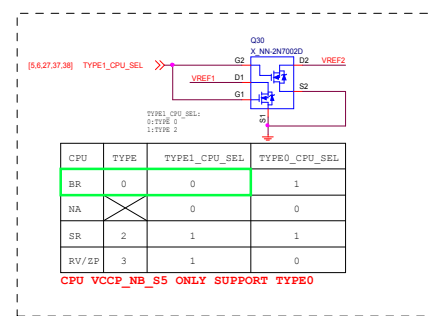
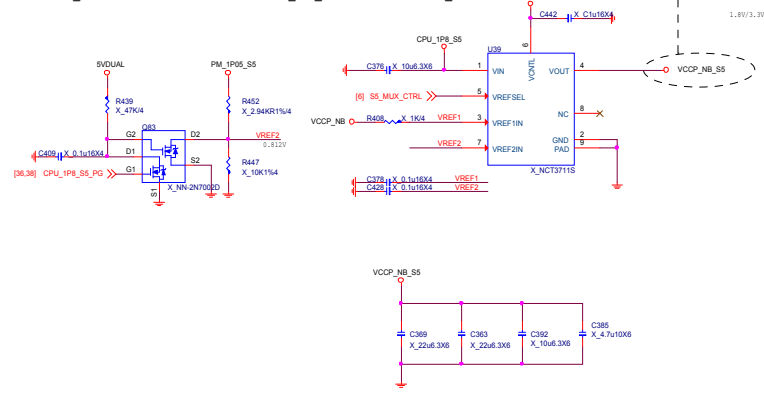


FOR
VCCP_SOC_S5
0.9A

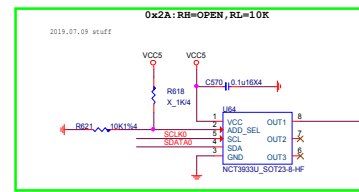
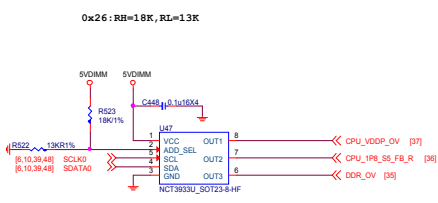
TYPE0 Only

S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_S0C<0.775V (OR 0.85V), VDDCR_SOC_S5 =0.775V.
If VDDCR_S0C >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB



Over Voltage Control IC

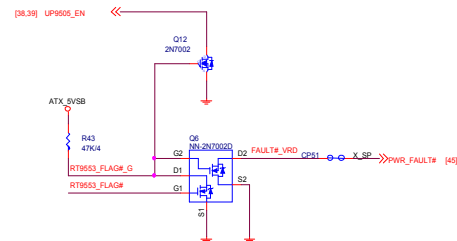


UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x2B	0x2C	0x2D	0x2E	0x2F
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%


MSI
Link to the Future
MICRO-START INTL CO.,LTD.
CPU Power NB Switch / NCT3933 OV
MS-7B84
Date: Friday, July 15, 2016
Sheet: 43 of 53

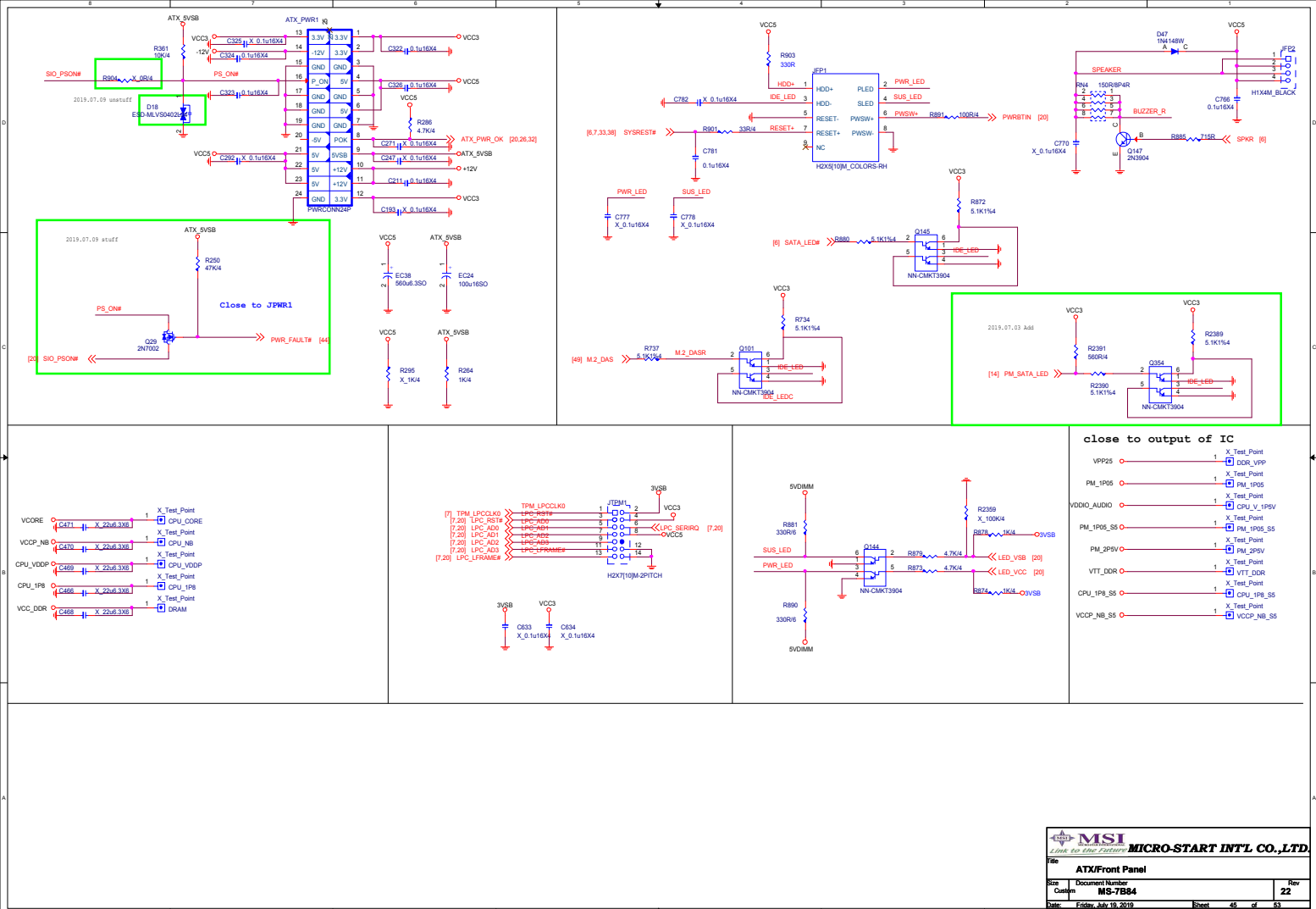
NB EDC MAX75A



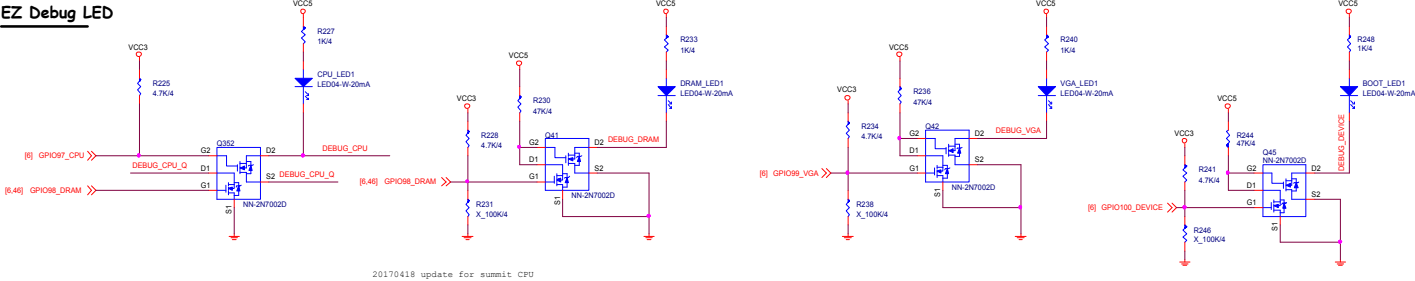
```
I3933_imon*[R17*R18/(R17+R18)]= Istep* Rdcr*100
I3933_imon= 10uA/step
Istep=4.785A
```

NB:
 $D = V_{out}/V_{in} = 1.4/12 = 0.1166$
 $N = \text{Phase number} = 2$
 $= 75A \cdot \sqrt{0.0583 - 0.0136}$
 $= 15.8A$

 MSI <small>Micro-Star International, Inc.</small> <i>Link to the Future</i>		MICRO-START INT'L CO.,LTD	
Title RT9553B CURRENT SENSE			
Size Custom	Document Number MS-7B84		Rev 22
Date: Friday, July 19, 2019	Sheet 44	of 53	



EZ Debug LED



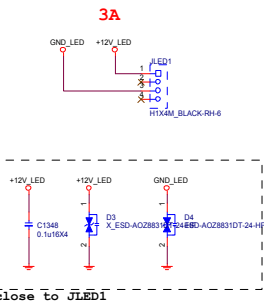
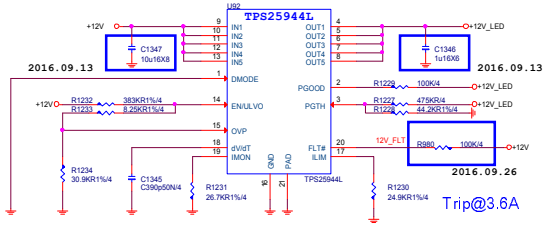
20170418 update for summit CPU

LED Control by SIO

JLED

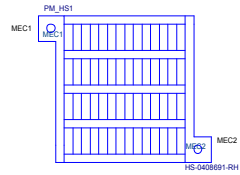
2016.07.06 Use TPS25944L

GPIO	GPIO97	GPIO98	GPIO99	GPIO100
GPIO PULL HIGH	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
GPO LOW	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

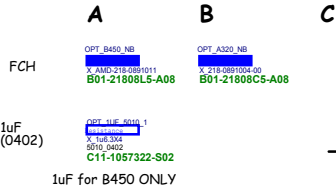


AM4 APU Detect LED Circuit

HEAT SINK



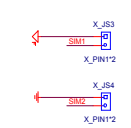
5010 Level



CPU Socket



Simulation

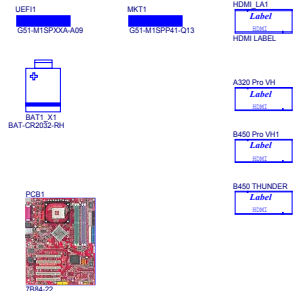


5020 Level



CAP USE N07 for A320/B450 SKU

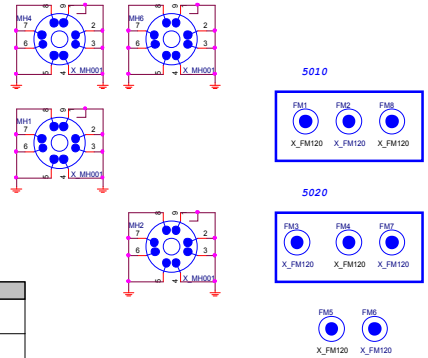
MANUAL PART



PK0-07B8422-G37, 精成-深圳, 22, 寶安恩斯邁廠 (MSIS)
PK0-07B8422-E48, 競華, 23, 寶安恩斯邁廠 (MSIS)

OPT	Configure	BOM	Function
		601-7B84-A01	XXXX

Optics Orientation Holes



MSI Link to the Future		MICRO-START INT'L CO., LTD.	
File BOM OPTION			
Size	Document Number	Rev	
Custom	MS-7B84	22	
Date: Friday, July 16, 2019		Sheet	47 of 53

3.3V@2.5A

